ITL.1059US
(P17918)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: ACCESSING DATA FROM DIFFERENT MEMORY LOCATIONS IN THE SAME CYCLE

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Express Mail No. EL 990 136 879 US

Date: November 19, 2003

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ACCESSING DATA FROM DIFFERENT MEMORY LOCATIONS IN THE SAME CYCLE

Background

This invention relates generally to digital signal processors.

A digital signal processor is an integrated circuit designed for high speed data manipulation. Digital signal processors may be used in audio, communications, image manipulation, and other data acquisition and data control applications.

Digital signal processors may use a modified Harvard architecture with dual ported memory where two data address buses are used to fetch data items from two different vectors located in memory at the same time. By accessing two data items at the same time, the computation units may be continuously fed with data. Dual ported memory is typically implemented using several banks of single ported memory. In such implementations, two data fetches may be done in one cycle when the data that must be accessed are in different memory banks that may be accessed at the same time.

As a result, when the data to be accessed is in the same memory bank, then this parallel processing is not possible. As a result, extra cycles may be required.

Thus, there is a need for better ways to access data in digital signal processing.

Brief Description of the Drawings

Figure 1 is an architectural level view of a digital signal processor in accordance with one embodiment of the present invention;

Figure 2 is a more detailed depiction of a portion of the embodiment shown in Figure 1 in accordance with one embodiment of the present invention;

Figure 3 is a flow chart for one embodiment of the present invention; and

Figure 4 is a schematic system depiction of one embodiment of the present invention.

Detailed Description

Referring to Figure 1, a digital signal processor 10 may include a system bus interface 12 coupled to an L1 data memory 14. The memory 14 may include ports coupled to the buses data 0 and data 1 which carry data back to a core 24. In a modified Harvard architecture, parallel memory accesses may be achieved using the buses DA0 and DA1 when data in different memory banks are targeted for data sought by the core 24.

The digital signal processor core 24 may have an address interface 26, a video processing unit 28, an accumulator 30, a shifter 32, a multiplier 34a, a multiplier 34b, and a pair of arithmetic logic units 36. The system bus interface 12 may also be coupled to an L1 instruction memory 38 which operates with a sequencer 40.

A memory controller 16 may include an address interface 18 and a pair of arithmetic logic units 20 and 22. The controller 16 receives the signals on LD0 and LD1 buses which provide data to the core 24. The controller 16 outputs addresses on the data buses DA0 and DA1. When different memory banks in the memory 14 are addressed by the core 24, the separate DA0 and DA1 buses may be utilized to address two locations at the same time in the same cycle.

Moreover, a controller 18 may be provided on the output of the controller 16 (or as part of the controller 16) between the data buses DA0 and DA1. The controller 18 may compare the addresses on buses DA0 and DA1 to see if they are directed to access the same memory subline. For example, a subline may be 64 bits while a line is 256 bits in one embodiment. If the targeted data is in the same subline, then a 64 bit read from the same or different 32 bit segments in the same subline may be implemented in the same cycle. The 64 bit read may be accomplished from the same subline at the same time, even though each of these accesses target the same memory bank.

The controller 18, in one embodiment, may include a comparator 42 that compares the addresses on the DA0 and DA1 buses as shown in Figure 2. If the same 64 bit subline is being addressed, and if 64 bit addressing is enabled (64b_ enabled), then the output of the AND gate 44 is provided to the 64 bit read port in the L1 data memory 14.

The 64 bit read port is simply the combination of the conventional ports 0 and 1 of a modified Harvard architecture. The ports 0 and 1 are used to address two locations in different memory banks in the memory 14 in the same cycle.

Different 32 bit segments of the same subline may be read at the same time in the same cycle when a signal is received by the 64 bit read port. A first 32 bit data output from the data memory 14 may be sent on data 0 and the other 32 bit data output may be provided on data 1. However, if each access is directed to the same 32 bit segment of the same subline, that same 32 bit segment may be provided on both data 0 and data 1.

Even in situations where the same memory bank is being accessed, it is possible nonetheless to do the read in the same cycle. Under the modified Harvard architecture this is not possible. As a result, the number of cycles that are utilized over a large number of read operations may be reduced in some embodiments of the present invention. In some embodiments, this improvement may be completely transparent to the instruction set architecture. However, the programmer can take advantage of this capability to get vector-like performance from traditional microprocessors.

While a hardware implementation is illustrated, a flow chart, shown in Figure 3, illustrates the operation of the hardware and further provides an illustration of a software based approach. In a software based approach, the code may

be stored in a processor-based controller 18, as one example, or the core 24, as another example.

In any case, an initial check at diamond 44 determines whether different memory banks are being accessed. If so, parallel read operations may be done to save cycles as indicated in block 48. However, even if different memory banks are not accessed, as determined in diamond 44, if the same subline would be accessed, as determined in diamond 46, the operation can proceed to read both segments in the same cycle.

Turning to Figure 4, a portion of a system 50 in accordance with an embodiment of the present invention is described. The system 50 may be used in wireless devices such as, for example, a personal digital assistant (PDA), a laptop or portable computer with wireless capability, a web tablet, a wireless telephone, a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit and/or receive information wirelessly. System 50 may be used in any of the following systems: a wireless local area network (WLAN) system, a wireless personal area network (WPAN) system, or a cellular network, although the scope of the present invention is not limited in this respect.

System 50 may include the digital signal processor 10, a general purpose processor 56, an input/output (I/O) device 56 (e.g. a keypad, display), a memory 60, and a wireless interface 58 and, coupled to each other via, a bus

54. It should be noted that the scope of the present invention is not limited to embodiments having any or all of these components.

The general purpose processor 52 may comprise, for example, one or more microprocessors, micro-controllers, or the like. Memory 60 may be used to store messages transmitted to or by system 50. Memory 60 may also optionally be used to store instructions that are executed by the processors 10 and 52 during the operation of system 50, and may be used to store user data. Memory 60 may be provided by one or more different types of memory. For example, memory 60 may comprise a volatile memory (any type of random access memory) or a non-volatile memory such as a flash memory.

The I/O device 56 may be used to generate a message. The system 50 may use the wireless interface 58 to transmit and receive messages to and from a wireless communication network with a radio frequency (RF) signal. Examples of the wireless interface 58 may include an antenna, or a wireless transceiver, such as a dipole antenna, although the scope of the present invention is not limited in this respect. Also, the I/O device 56 may deliver a voltage reflecting what is stored as either a digital output (if digital information was stored), or it may be analog information (if analog information was stored).

While an example is provided of a line of 256 bits, a subline of 64 bits and two 32 bit portions thereof, the

present invention is not limited to embodiments with any particular number of bits per line and portion of a line.

While an example in a wireless application is provided above, embodiments of the present invention may also be used in non-wireless applications as well.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is: